ELEC 3004 DIGITAL SYSTEMS 2

Credit Points 10

Legacy Code 300019

Coordinator Qi Cheng (https://directory.westernsydney.edu.au/search/name/Qi Cheng/)

Description This subject covers modern logic design techniques and the process of creating logic circuits and systems from design specifications to implementation. Topics include logic design techniques for combinational and sequential logic circuits; hardware description language (HDL); logic circuit implementation using an HDL; state-of-the-art logic circuit design tools; and programmable logic devices.

School Eng, Design & Built Env

Discipline Communications Technologies

Student Contribution Band HECS Band 2 10cp

Check your fees via the Fees (https://www.westernsydney.edu.au/currentstudents/current_students/fees/) page.

Level Undergraduate Level 3 subject

Pre-requisite(s) ELEC 1001

Learning Outcomes

On successful completion of this subject, students should be able to:

1. Describe functions of encoders/decoders, adders/subtractors, multiplexers/demultiplexers and their design procedures; and design them using VHDL (combinational logic)
2. Describe functions of flip-flops, registers, counters, finite-state machines and their design procedures; and design them using VHDL (sequential logic)
3. Build ALUs using VHDL
4. Describe VHDL memory functions and use them to design RAM units
5. Describe VHDL bus and I/O functions and use them to design bidirectional bus and tri-state buses
6. Implement logic circuits on FPGA boards

Subject Content

Logic function optimization
State diagram, state table
Logic circuit design
Hardware description languages (VHDL)
Statements, structures, data, variable, signal, type
Logic circuit modelling using VHDL
RAM implementation
Bus implementation
ALU implementation
Field programmable gate array devices
Implementation of logic circuits on FPGA

Assessment

The following table summarises the standard assessment tasks for this subject. Please note this is a guide only. Assessment tasks are regularly updated, where there is a difference your Learning Guide takes precedence.

Type	Length	Percent	Threshold	Individual/ Group Task	Mandatory
Numerical Problem Solving	Approximately 10 questions each, individual theoretical and programming tasks	15	N	Individual	Y
Practical	3 hours per session/ Approximat 5-10 pages	20	N	Individual	Y
Final Exam	2 hours	65	N	Individual	Y

Teaching Periods

Sydney City Campus - Term 3 (2024)

Sydney City

On-site

Subject Contact Ehsan Gatavi (https://directory.westernsydney.edu.au/search/name/Ehsan Gatavi/)

View timetable (https://classregistration.westernsydney.edu.au/even/timetable/?subject_code=ELEC3004_24-SC3_SC_1#subjects)

Sydney City Campus - Term 2 (2025)

Sydney City

On-site

Subject Contact Ehsan Gatavi (https://directory.westernsydney.edu.au/search/name/Ehsan Gatavi/)

View timetable (https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC3004_25-SC2_SC_1#subjects)

Spring (2025)

Penrith (Kingswood)

Hybrid

Subject Contact Qi Cheng (https://directory.westernsydney.edu.au/search/name/Qi Cheng/)

View timetable (https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC3004_25-SPR_KW_3#subjects)

Parramatta City - Macquarie St

Hybrid

Subject Contact Qi Cheng (https://directory.westernsydney.edu.au/search/name/Qi Cheng/)

View timetable (https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC3004_25-SPR_PC_3#subjects)