

# ELEC 1001 DIGITAL SYSTEMS 1

**Credit Points** 10

**Legacy Code** 300018

**Coordinator** Peter Lendrum ([https://directory.westernsydney.edu.au/search/name/Peter Lendrum/](https://directory.westernsydney.edu.au/search/name/Peter%20Lendrum/))

**Description** This subject provides students with a solid background in digital logic design which is foundational to the fields of electrical and computer engineering. Digital logic design involves building electronic components and hardware, such as circuit boards and microchip processors. Students are first introduced to the fundamentals of digital logic, basic logic devices and Boolean algebra. This is followed by analysis and design of combinational and sequential logic circuits.

**School** Eng, Design & Built Env

**Discipline** Communications Technologies

**Student Contribution Band** HECS Band 2 10cp

Check your HECS Band contribution amount via the Fees ([https://www.westernsydney.edu.au/currentstudents/current\\_students/fees/](https://www.westernsydney.edu.au/currentstudents/current_students/fees/)) page.

**Level** Undergraduate Level 1 subject

**Equivalent Subjects** ELEC 1002 - Digital Systems 1 (WSTC AssocD)

**Assumed Knowledge**

Knowledge on basic principles of analysing an electric circuit, Kirchhoff's Voltage and Current laws and their use in electric circuits and concept of operational amplifier and its circuit would be desirable.

## Learning Outcomes

On successful completion of this subject, students should be able to:

1. Describe basic digital concepts and the operation of basic logic gates.
2. Apply Boolean Algebra to a range of logic expressions
3. Apply Karnaugh maps to a range of logic expressions.
4. Analyse and design combinational logic circuits.
5. Describe the operation of a range of memory devices.
6. Describe the principles of analogue-to-digital and digital-to-analogue conversion schemes.

## Subject Content

1. Boolean algebra and logic simplification
2. Karnaugh maps
3. Combinational logic circuits
4. Flip-flops, counters, registers
5. Memory
6. Analogue-to-digital and digital-to-analogue conversion

## Assessment

The following table summarises the standard assessment tasks for this subject. Please note this is a guide only. Assessment tasks are regularly updated, where there is a difference your Learning Guide takes precedence.

Type	Length	Percent	Threshold	Individual/ Group Task
Practical	3 hours (per Practical)	20	N	Individual
Intra-session Exam	1 hour	20	N	Individual
Final Exam	2 hours	60	N	Individual

Prescribed Texts

Floyd, T. L. (2015). Digital fundamentals. 11th Global ed, Boston, Mass: Pearson Education Inc

Teaching Periods

## Autumn (2022) Penrith (Kingswood)

**Day**

**Subject Contact** Qi Cheng ([https://directory.westernsydney.edu.au/search/name/Qi Cheng/](https://directory.westernsydney.edu.au/search/name/Qi%20Cheng/))

View timetable ([https://classregistration.westernsydney.edu.au/even/timetable/?subject\\_code=ELEC1001\\_22-AUT\\_KW\\_D#subjects](https://classregistration.westernsydney.edu.au/even/timetable/?subject_code=ELEC1001_22-AUT_KW_D#subjects))

## Parramatta - Victoria Rd

**Day**

**Subject Contact** Qi Cheng ([https://directory.westernsydney.edu.au/search/name/Qi Cheng/](https://directory.westernsydney.edu.au/search/name/Qi%20Cheng/))

View timetable ([https://classregistration.westernsydney.edu.au/even/timetable/?subject\\_code=ELEC1001\\_22-AUT\\_PS\\_D#subjects](https://classregistration.westernsydney.edu.au/even/timetable/?subject_code=ELEC1001_22-AUT_PS_D#subjects))

## Sydney City Campus - Term 2 (2022) Sydney City

**Day**

**Subject Contact** Peter Lendrum ([https://directory.westernsydney.edu.au/search/name/Peter Lendrum/](https://directory.westernsydney.edu.au/search/name/Peter%20Lendrum/))

View timetable ([https://classregistration.westernsydney.edu.au/even/timetable/?subject\\_code=ELEC1001\\_22-SC2\\_SC\\_D#subjects](https://classregistration.westernsydney.edu.au/even/timetable/?subject_code=ELEC1001_22-SC2_SC_D#subjects))

## Autumn (2023) Penrith (Kingswood)

**On-site**

**Subject Contact** Qi Cheng ([https://directory.westernsydney.edu.au/search/name/Qi Cheng/](https://directory.westernsydney.edu.au/search/name/Qi%20Cheng/))

View timetable ([https://classregistration.westernsydney.edu.au/odd/timetable/?subject\\_code=ELEC1001\\_23-AUT\\_KW\\_1#subjects](https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC1001_23-AUT_KW_1#subjects))

## Parramatta City - Macquarie St

**On-site**

**Subject Contact** Peter Lendrum ([https://directory.westernsydney.edu.au/search/name/Peter Lendrum/](https://directory.westernsydney.edu.au/search/name/Peter%20Lendrum/))

View timetable ([https://classregistration.westernsydney.edu.au/odd/timetable/?subject\\_code=ELEC1001\\_23-AUT\\_PC\\_1#subjects](https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC1001_23-AUT_PC_1#subjects))

## Sydney City Campus - Term 1 (2023) Sydney City

**On-site**

**Subject Contact** Peter Lendrum ([https://directory.westernsydney.edu.au/search/name/Peter Lendrum/](https://directory.westernsydney.edu.au/search/name/Peter%20Lendrum/))

View timetable ([https://classregistration.westernsydney.edu.au/odd/timetable/?subject\\_code=ELEC1001\\_23-SC1\\_SC\\_1#subjects](https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC1001_23-SC1_SC_1#subjects))

## **Sydney City Campus - Term 3 (2023)**

### **Sydney City**

#### **On-site**

**Subject Contact** Peter Lendrum ([https://directory.westernsydney.edu.au/search/name/Peter Lendrum/](https://directory.westernsydney.edu.au/search/name/Peter%20Lendrum/))

View timetable ([https://classregistration.westernsydney.edu.au/odd/timetable/?subject\\_code=ELEC1001\\_23-SC3\\_SC\\_1#subjects](https://classregistration.westernsydney.edu.au/odd/timetable/?subject_code=ELEC1001_23-SC3_SC_1#subjects))